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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/928,975	HERNER ET AL.
	Examiner	Art Unit
	Thomas J. Magee	2811

-- The MAILING DATE of this communicati n appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 12 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (US 2002/0045342 A1) in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits,"Noyes Publ.,Westwood, New Jersey (1993), pp. 44 – 50), Nakayama et al. ("Excellent Process Control Technology for Highly Manufacturable And High Performance 0.18 um CMOS LSIs," IEEE Digest of Technical Papers, Symposium on VLSI Technology (1998), pp. 146 – 147) and Spinelli et al. ("An improved Formula for the Determination of the Polysilicon Doping," IEEE Electron Device Letters, Vol. 22, No. 6, (June, 2001) pp. 281 – 283).

Hu et al. disclose a device (with line widths < 0.25 um) (Abstract; p.2, par. [0013, p.3, par. [0034], p. 1, par. [0031]) comprising: a first (doped) silicon layer (214) (Figure 2E) deposited atop a (second) silicon layer (216) with incorporated dopants (1 x 10(^)18 to 5 x 10(^)21 atoms/cm(^)3) (page 7, lines 11 – 13) and an overlying titanium layer (218), which, after annealing forms low resistivity C54 titanium silicide. Hu et al. do not explicitly disclose the doping concentration of the first silicon layer, but typical doping of silicon over gate

oxides is in the range, 10(^)19 to 10(^)20/cm(^)3 (See for example, Spinelli et al., page 282, Figure 2). Hu et al. do not explicitly disclose the thickness ratio for the silicon/titanium layers, but this can be calculated from the disclosed value for the titanium silicide thickness (approximately 1000 Angstroms) (p.4, right side, top). It is extremely well known in the art (Wilson et al., p. 44, bottom par.) that approximately 1 Angstrom Ti + 2.27 Angstroms Si produces 2.51 Angstroms TiSi2. Hence for complete reaction and in order to consume the Ti in a reaction producing 1000 Angstroms TiSi2, at a minimum, it is necessary to have a titanium layer of approximately 400 Angstroms thickness and a silicon layer of approximately 900 Angstroms thickness, wherein, $t1 \geq 2.0$ (t2)

Further, Hu et al. stress the importance of both grain size and nucleation sites as determinants of resistivity and "fine line effect." This result is affirmed by Wilson et al., who disclose (See Figure 16) that the sheet resistance of titanium silicide (formed by annealing) as a function of initial Ti layer thickness decreases rapidly and reaches a relatively saturated zone for thicknesses > 700 Angstroms, where sheet resistances are less than 3 ohms/square for t greater than approximately 500 Angstroms. Since, in this case, the substrate thickness, t1, is large with respect to the layer thickness, t2, there is no apparent (t1/t2) dependence and the results are almost identical to the graphical data recited by Applicant. Furthermore, if the ratio, t1/t2, is small, it would be obvious that all of the Si would be consumed during annealing, thereby forming a stable titanium silicide contact of low contact resistance.

Additionally, Nakayama et al. disclose for 0.18 and 0.25 um lines that the low sheet resistance (less than 2 ohms/square) associated with uniform titanium silicide (C54) formation can be obtained with no fine line effect. Using Figure 4, the thickness of the reacted silicide layer is less than 1000 Angstroms. Based on the calculation above, $t1 \geq 2\,(t2)$. Hence, the attainment of low sheet resistance titanium silicide layers of small line width with $t1 \geq 2(t2)$ is considered a product-by-process limitation. "Even though product-by-process claims are limited and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

4. Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. in view of Wilson et al., Nakayama et al., and Spinelli et al., as applied to Claim 1 above.

There is no statistical difference between values of t1 equal to 2.2(t2) and 2.3(t2) +/- 0.1(t2), hence these claims, as recited, are overlapping and redundant. Further, Hu et al. utilize thicknesses that are comparable to values recited in Claim 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the silicide layer using the claimed thicknesses of silicon and titanium, since it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al., in view of Wilson et al., Nakayama et al., and Spinelli et al., as applied to Claim 1. Hu et al.disclose (page 2, right side, last paragraph) the use of doped silicon or poly-silicon in the first semiconductor region. Although Hu et al. do not disclose the volume concentration or the dopant, it is commonly known that boron is used as a p-type dopant and it would be obvious to one of ordinary skill in the art to deploy a boron-doped layer to obtain a p-doped material in the word line stack.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. in view of Wilson et al., Nakayama et al., and Spinelli et al.
As discussed earlier, the deployment of first silicon regions of doping concentrations in The range of 10(^)20/cm(^)3 is routine in the art for gate structures (Spinelli et al., Figure 2)
Hu et al. disclose a structure of approximately 0.25 um in width (Abstract; p. 2, par. [0013], p. 3, par. [0034], p. 1, par. [0031]) having a doped first semiconductor region and titanium silicide conductors overlying the first semiconductor region that are all in the low resistivity C54 phase. Although Hu et al. do not disclose the sheet resistances of the Ohmic contacts, it is known (Wilson et al.) for a C54 phase titanium silicide layer that for a range of thicknesses, the sheet resistances will be less than 3 ohms/square. Similarly, Nakayama et al.

disclose (Figure 5) for structures of 0.15 and 0.25 um width, and t1 > 2 (t2), sheet resistances below 2.0 ohms/square. Hence, the attainment of low sheet resistance titanium silicide layers of small line width is considered a product-by-process limitation. "Even though product-by-process claims are limited and defined by the process, determination of patentability is based on the pro- duct itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. in view of Wilson et al., Nakayama et al., and Spinelli et al., as applied to Claim 1, and further in view of Tsukude et al. ("A 256Mb DRAM," Advance Magazine, Mitsubishi Electric (June, 1996) Vol. 75, pp. 5 – 8).

Hu et al. disclose ([0002 through [0004]) that the structure comprises a memory array with stacked layers in the word line. However, it would be obvious that other circuit elements are required to complete an integrated circuit, including bit lines, associated passive components and interconnections, all of which would be stacked in a vertical 3-D sequence, because of limited area. It has been well established in the art (See Tsukude et al., p.5) that DRAM devices with a 0.25 um design rule effectively utilize a stacked memory cell architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tsukude et al. with Hu et al.,

Wilson et al., Nakayama et al., and Spinelli et al. to produce a complete working device.

Response to Arguments

8. Applicant's arguments in regard to Claims 1 – 8 have been carefully considered, but have been found to be unpersuasive. Applicant has stated that the primary reference does not disclose that line widths are < 0.25 um. This is incorrect and the reference clearly discloses that widths < 0.25 um have been used and demonstrated to produce superior results, as discussed above. Hu et al. also clearly disclose (claim 1) the use of a titanium layer. In response to Applicant's argument that Spinelli et al. does not disclose the claimed structure of Applicant, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Claim 1 recited in the instant application recites the reaction of a layer with a semiconductor region "to form titanium disilicide" with a line width of approximately 0.3 um and with appropriate t1, t2 values, whereupon, after annealing, the disilicide has a sheet resistance of < 3 ohms/square. This is most clearly a structure (product) produced by a process. Nakayama discloses the limitations of Claim 1 and produces smaller gates using another limitation with no fine line effect.

Wilson et al. is used to affirm Hu et al., as was stated and to further disclose that another factor is controlling resistivity. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusions

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305**

5396. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Thomas Magee
July 20, 2003

TOM THOMAS
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